Specification

The Action notes that the application refers to subject matter disclosed in prior co-pending Application no. 09/052,895 and 09/052,915, filed March 31, 1998. The Action then states that a reference to the prior applications must be inserted as the first sentence of the specification of this application. Applicants respectfully disagree, and point out that the applications referred to are not being relied upon for priority. Rather, the subject matter of the applications referred to is being incorporated by reference under MPEP 608.01(p), which does not require a reference be inserted as the first sentence of the application.

Rejection of Claims 15-57 under 35 U.S.C. § 102(e)

The Action rejects claims 15-57 under 35 U.S.C. § 102(e) as being anticipated by Chen. Applicants respectfully submit the claims in their present form are allowable over the cited art and traverse the rejections. For a 102(e) rejection to be proper, the cited art must show each and every element as set forth in a claim. (*See* MPEP § 2131.01.)

Claim 15

Claim 15 is directed towards a method for measuring cross-coupling capacitance and stands rejected under 35 U.S.C. § 102(e) as being anticipated by Chen. Applicants traverse the rejection. The Action states that the features of claim 15 are shown in the background section, column 3 and columns 5-7 of Chen.

The method described in Chen for measuring cross-coupling capacitance does not teach or suggest the method disclosed in claim 15. Referring to Figure 1, Chen describes a test structure for measuring cross-coupling capacitance that connects a test wire 105 to a node between a first pair of transistors 119 and 120 and a target wire 106-n to a node between a second pair of transistors 112 and 113. Each pair of transistors is used to selectively charge or discharge the test 105 and target 106-n wires. In columns 5-7, Chen describes using this structure to measure the cross-coupling capacitance between the test wire 105 and target wire 106-n. First, both the test 105 and target 106-n wires are discharged during a reset phase (columns 5-6, lines 60-5). Then during an enabling stage, the target wire 106-n is charged (column 6, lines 15-23). A measuring stage then charges the test wire 105 and a measure of the current I_{chargl} from the target wire 106-n to ground, through transistor 112, is measured using ammeter 138 (column 6 lines 24-44). The measurement of this current

continues while charging of the test wire 105 is discontinued to ensure all charge on the target wire 106-n has been measured (column 6, lines 44-56). Finally, measurement stops when all transistors are turned off and the process is repeated a number of times. The average current over the time period of measurement yields the cross-coupling capacitance c_n between the test 105 and target 106-n wires according to equation 2 of Chen.

In summary, Chen uses a circuit with two pairs of transistors connected to each of a test wire 105 and target wire 106-n to control charging of the two wires. The method in Chen suggests discharging both wires, charging a first wire (the target wire 106-n), then charging a second wire (the test wire 105), and taking a measurement of current while both are charged, and continuing measurement while the charging source V_{dd} is no longer connected to the second wire. The capacitance between the two wires is then computed from the measured current.

Additionally, the background section of Chen describes a prior art method for measuring cross-coupling capacitance that consists of both a test and reference structure, and "[t]he difference in current between charging (or discharging) the total capacitance of the reference and target structures is then used to compute a measurement of the target interconnect capacitance."

By contrast to both these methods, claim 15 recites a method wherein a first measurement associated with the capacitance of the first wire is made after the first wire is charged, and another measurement associated with the capacitance of the first wire is made after the first and second wires have been charged. Therefore, claim 15 recites a method wherein *two measurements associated with the capacitance of a first wire are made*. Claim 15 specifically recites, "performing a first measurement associated with a capacitance of the first wire," "performing a second measurement associated with a capacitance of the first wire," and "calculating a difference between the first and second measurements to determine the cross-coupling capacitance between the first and second wires."

The method in Chen suggests only taking a *single measurement* of current. Using a single measurement of current necessitates the much more complex clock circuitry as well as a pair of transistors connected to both the test wire (transistors 119 and 120) and target wire (transistors 112 and 113), as shown in Figure 1 of Chen. Therefore, the method of Chen does not suggest taking *two measurements associated with the capacitance of a single wire* as a means for measuring cross-coupling capacitance as recited in claim15.

Additionally, the background section of Chen only refers to a prior art method, also disclosed in the present application's background section, that involves taking measurements of capacitance of *two separate test structures*. Therefore, the two measurements cannot be associated with the capacitance of a single wire and cannot suggest taking *two measurements associated with the capacitance of a single wire* as a means for measuring cross-coupling capacitance as recited in claim15.

Since the cited reference fails to describe at least one element recited in claim 15, Applicants believe the claim is not subject to a 102(e) rejection and is therefore in condition for allowance. Claims 2-34, which depend from claim 1, should also be allowable for at least the same reasons, as well as for the respective additional elements recited therein.

<u>Claims 35</u>

Claim 35 is directed towards a circuit for measuring cross-coupling capacitance and stands rejected under 35 U.S.C. § 102(e) as being anticipated by Chen. Applicants traverse the rejection. The Action states that the features of claim 35 are shown in Figure 1, column 3, and columns 5-7 of Chen.

Claim 35 recites in part, "wherein the cross-coupling capacitance is measured between the first and second wires by subtracting two capacitance-related measurements associated with the first wire, one of the measurements being performed with the second wire at a first voltage level and the other of the measurements being performed with the second wire charged to a second voltage level."

This feature is not shown by Chen as discussed with respect to claim 15. Chen describes taking a single measurement of current in order to measure cross-coupling capacitance. By contrast, claim 35 describes taking a first measurement associated with the first wire, taking a second measurement associated with the first wire, and measuring the cross-coupling capacitance by subtracting the two measurements.

Since the cited reference fails to describe at least one element recited in claim 35, Applicants believe the claim is not subject to a 102(e) rejection and is therefore in condition for allowance. Claims 36-46, which depend from claim 35, should also be allowable for at least the same reasons, as well as for the respective additional elements recited therein.

Claim 47 and 51

Claims 47 is directed towards a circuit for calculating cross-coupling capacitance and stands rejected under 35 U.S.C. § 102(e) as being anticipated by Chen. Claim 47 recites in part, "means for calculating cross-coupling capacitance by measuring charge needed to charge the first wire to a predetermined voltage with the second wire grounded and measuring charge needed to charge the first wire to the predetermined voltage with the second wire charged to the predetermined voltage and taking a difference between the two measurements."

Claim 51 is directed towards a method for determining cross-coupling capacitance and also stands rejected under 35 U.S.C. § 102(e) as being anticipated by Chen. Claim 51 recites in part, "measuring a first charge that is deposited on the first wire over the period of time, the first charge being measured each time the second wire is grounded." Applicants traverse the rejections. Chen fails to show these features for similar reasons as discussed with respect to claims 15 and 35 above.

Since the cited reference fails to describe at least one element recited in claims 47 and 51, Applicants believe the claims are not subject to a 102(e) rejection and are therefore in condition for allowance. Claims 48-50 and 51-57, which depend from claims 47 and 51, respectively, should also be allowable for at least the same reasons, as well as for the respective additional elements recited therein.

CONCLUSION

The claims in their present form should be allowable. Such action is respectfully requested.

Respectfully submitted,

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Marked-up Version of Amended Specification
Pursuant to 37 C.F.R. §§ 1.121(b)

Please replace the paragraph beginning at page 5, line 18 with the following paragraph:

Figure 7 [8] is a block diagram illustrating an overview of an IC design simulation tool.

Please replace the paragraph beginning at page 6, line 1 with the following paragraph:

Figure 8 [9] is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention.

Please replace the paragraph beginning at page 6, line 4 with the following paragraph:

Figure 9 [10] is one embodiment of a computer system suitable for use with the invention.

Please replace the paragraph beginning at page 12, line 5 with the following paragraph:

Figure 7 [8] is a block diagram illustrating an overview of an IC design simulation tool. As illustrated, IC design simulation tool 700 [800] is constituted with design reader 702 [802], static partitioner 703 [803] and simulation engine 704 [804] comprising dynamic partitioner 707 [807], scheduler 709 [809], node evaluator 708 [808] and model evaluators 706 [806]. The elements are operatively coupled to each other as shown. Design reader 702 [802] and some model evaluators 706 [806], in particular a transistor model evaluator and a wire model evaluator, are incorporated with the teachings of the present invention. Certain aspects of static partitioner 703 [803], dynamic partitioner 707 [807] and scheduler 709 [809] are the subject of co-pending U.S. Patent application number 09/333,124, filed June 14, 1999, and entitled "CIRCUIT SIMULATION USING DYNAMIC PARTITION AND ON-DEMAND EVALUATION" which is hereby fully incorporated by reference.

Please replace the paragraph beginning at page 12, line 20 with the following paragraph:

Design reader 702 [802] is used to read design description 710 [810] provided by a designer. Design description 710 [810] includes connectivity information connecting various models modeling electronic devices in the IC design. In one embodiment, in addition to flattening a hierarchical design, design reader 702 [802], also assigns device characterizations to selected ones of the electronic devices of the IC design. In one embodiment the device characterizations are determined as described above. Static partitioner 703 [803] pre-compiles or pre-partitions the IC design into static partitions as well as pre-processes the static partitions into a form particularly suitable for the dynamic partitioner 707 [807].

Please replace the paragraph beginning at page 13, line 5 with the following paragraph:

During simulation, dynamic partitioner 707 [807] further forms and re-forms dynamic partitions of the IC design that are relevant, referencing the pre-formed static partitions. Scheduler 709 [809] determines whether evaluations are necessary for the dynamic partitions for the particular simulation time step, and schedules the dynamic partitions for evaluation on an as-needed or on-demand basis. Accordingly, node evaluator 708 [808] and model evaluators 706 [806] are selectively invoked on an as-needed or on-demand basis to evaluate the states of the connections connecting the models, and various parameter values of the models, such as current, voltage and so forth, respectively.

Please replace the paragraph beginning at page 14, line 1 with the following paragraph:

Figure 8 [9] is a block diagram illustrating one embodiment of a parasitic extraction tool suitable for use with the present invention. As illustrated, the present invention includes parasitic extraction tool (PEX) 802 [902] and parasitic database (PDB) 804 [904]. PEX 802 [902] generates electrical modeling data for layout nets of an IC design, e.g. a deep sub-micron IC design, and stores the generated electrical modeling data in PDB 804 [904] for use by client applications, such as post layout analysis applications 818 [918]. Examples of post-layout analysis applications 818 [918] include Delay Calculator by Ultima Technology of Sunnyvale, CA, and Path Mill and Time Mill by Synopsis Inc. of Mountain View, CA.

Please replace the paragraph beginning at page 14, line 9 with the following paragraph:

PEX 802 [902] generates the electrical modeling data for the layout nets using extracted connectivity and geometrical data of the layout nets. In one embodiment PEX 802 [902] generates capacitive modeling data as described above. As shown, PEX 802 [902] includes read function 806 [906] that operates to input these connectivity and geometrical data of the layout nets. For the illustrated embodiment, the extracted connectivity and geometrical data of the layout nets are input from filtered databases (FDB) 816 [916].

Please replace the paragraph beginning at page 14, line 15 with the following paragraph:

The extracted connectivity and geometrical data are stored in FDB 816 [916] by layout cell hierarchies, one FDB per layout cell hierarchy, and indexed by layout nets. The connectivity and geometrical data were extracted at least in part in accordance with specified parasitic effect windows of the various layers of the IC design. Read function 806 [906] operates to retrieve the connectivity and geometrical data of the layout nets from FDB 816 [916] using the stored layout net indices. FDB 816 [916] is the subject of co-pending U.S. Patent application number 09/052,895, filed March 31, 1998, and entitled "METHOD AND APPARATUS FOR EXTRACTING AND STORING CONNECTIVITY AND GEOMETRICAL DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference.

Please replace the paragraph beginning at page 15, line 3 with the following paragraph:

PDB 804 [904] is designed to accommodate a large volume of electrical modeling data and concurrent accesses by multiple client applications, which is typically of today's and future deep sub-micron IC designs and design environments. For the illustrated embodiment, PDB 804 [904] has physical organization 814 [914] that allows a large volume of electrical modeling data to be stored in multiple physical media, and application interface 810 [910] that shields physical organization 814 [914] from PDB users, e.g. PEX 802 [902] and post layout analysis applications 818 [918]. Additionally, PDB 802 [902] has logical organization 812 [912] that abstracts physical organization 814 [914] to facilitate implementation of application interface 810 [910].

Please replace the paragraph beginning at page 15, line 12 with the following paragraph:

For the illustrated embodiment, PEX 802 [902] includes write function 808 [908] that operates to store the generated electrical modeling data of the layout nets into PDB 804 [904] using application interface 810 [910]. In alternate embodiments, write function 808 [908] may store the generated electrical modeling data of the layout nets using either logical and/or physical organizations 812-814 [912-914]. Similarly, selected ones of the client applications, e.g. post-layout analysis applications 818 [918], may also elect to access PDB 804 [904] through logical and/or physical organizations 812-814 [912-914].

Please replace the paragraph beginning at page 15, line 19 with the following paragraph:

Read function 806 [906] and write function 808 [908] are the subject of co-pending U.S. Patent application number 09/052,915, filed March 31, 1998 and entitled "METHOD AND APARATUS FOR GENERATING AND MAINTAINING ELECTRICAL MODELING DATA FOR A DEEP SUB-MICRON INTEGRATED CIRCUIT DESIGN," which is assigned to the corporate assignee of the present invention. The co-pending application is hereby fully incorporated by reference. Except for read function 806 [906] and write function 808 [908], PEX 802 [902] is intended to represent a broad category of electrical modeling tools known in the art. Examples of these electrical modeling tools include but not limited to Pattern Engine of xCalibre by Mentor Graphics, Columbus by Frequency Technology of San Jose, CA, and Arcadia by Synopsis.

Please replace the paragraph beginning at page 16, line 6 with the following paragraph:

Figure 9 [10] is one embodiment of a computer system suitable for use with the invention. Computer system 900 [1000] can be used, for example, for extraction and/or modeling of integrated circuits using the teachings of the present invention. Computer system 900 [1000] includes bus 901 [1001] or other communication device to communicate information and processor 902 [1002] coupled to bus 901 [1001] to process information. While computer system 900 [1000] is illustrated with a single processor, computer system 900 [100] can include multiple processors and/or co-processors. Computer system 900 [1000] further includes random access memory (RAM) or other dynamic storage device 904 [1004] (referred to as main memory), coupled to bus 901 [1001] to store information and instructions to be executed by processor 902 [1002]. Main memory

904 [1004] also can be used to store temporary variables or other intermediate information during execution of instructions by processor 902 [1002].

Please replace the paragraph beginning at page 16, line 17 with the following paragraph:

Computer system 900 [1000] also includes read only memory (ROM) and/or other static storage device 906 [1006] coupled to bus 901 [1001] to store static information and instructions for processor 902 [1002]. Data storage device 907 [1007] is coupled to bus 901 [1001] to store information and instructions. Data storage device 907 [1007] such as a magnetic disk or optical disc and corresponding drive can be coupled to computer system 900 [1000].

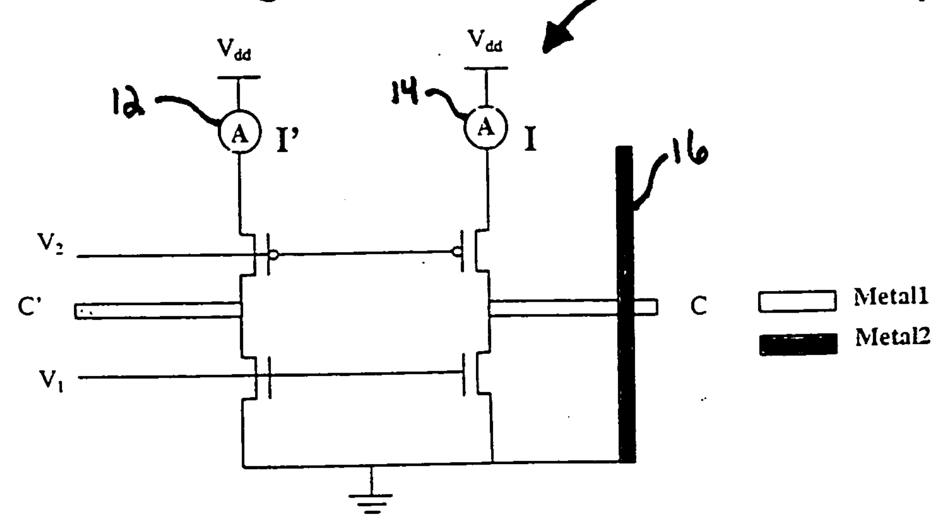
Please replace the paragraph beginning at page 16, line 22 with the following paragraph:

Computer system 900 [100] can also be coupled via bus 901 [1001] to display device 921 [1021], such as a cathode ray tube (CRT) or liquid crystal display (LCD), to display information to a computer user. Alphanumeric input device 922 [1022], including alphanumeric and other keys, is typically coupled to bus 901 [1001] to communicate information and command selections to processor 902 [1002]. Another type of user input device is cursor control 923 [1023], such as a mouse, a trackball, or cursor direction keys to communicate direction information and command selections to processor 902 [1002] and to control cursor movement on display 921 [1021].

Please replace the paragraph beginning at page 17, line 6 with the following paragraph:

According to one embodiment, extraction and/or modeling can be performed by computer system 900 [1000] in response to processor 902 [1002] executing sequences of instructions contained in main memory 904 [1004]. Instructions are provided to main memory 904 [1004] from a storage device, such as magnetic disk, a read-only memory (ROM) integrated circuit (IC), CD-ROM, DVD, via a remote connection (e.g., over a network), etc. In alternative embodiments, hard-wired circuitry can be used in place of or in combination with software instructions to implement the present invention. Thus, the present invention is not limited to any specific combination of hardware circuitry and software instructions.

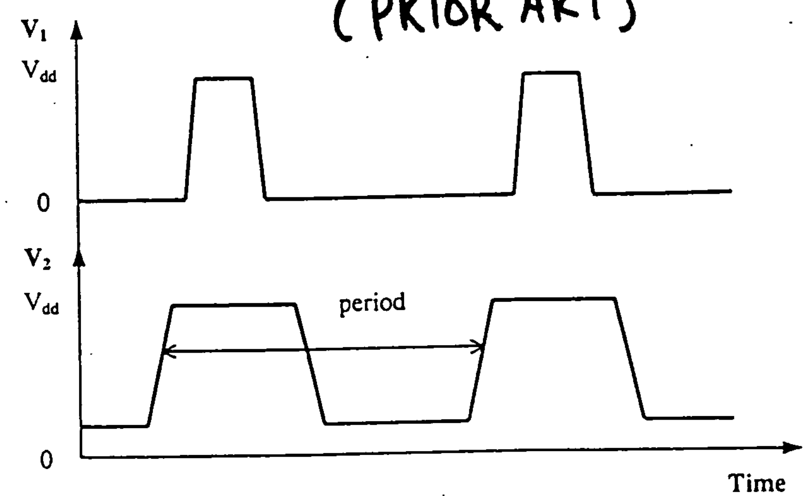
FIG. 1
(PRIOR ART)



~~FIG. 1~~

~~(PRIOR ART)~~

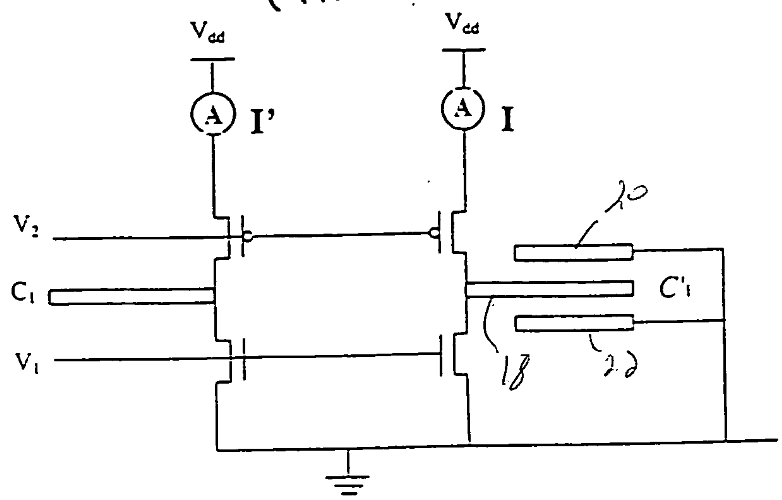
FIG. 2
(PRIOR ART)



~~FIG. 2~~

~~(PRIOR ART)~~

FIG. 3
(PRIOR ART)



~~FIG. 3 (PRIOR ART)~~

FIG. 4

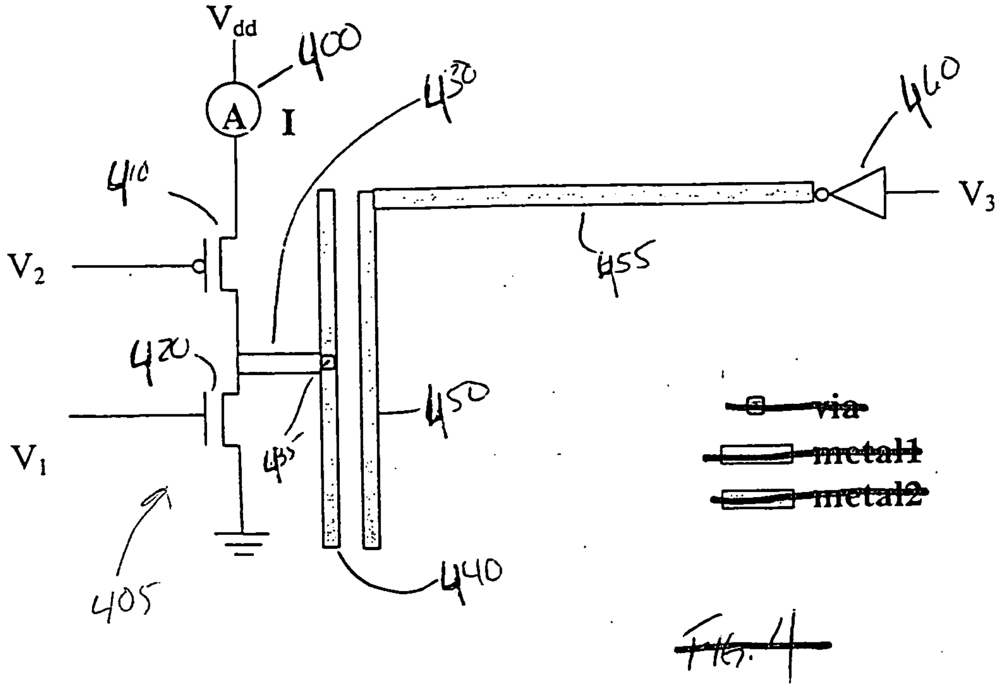
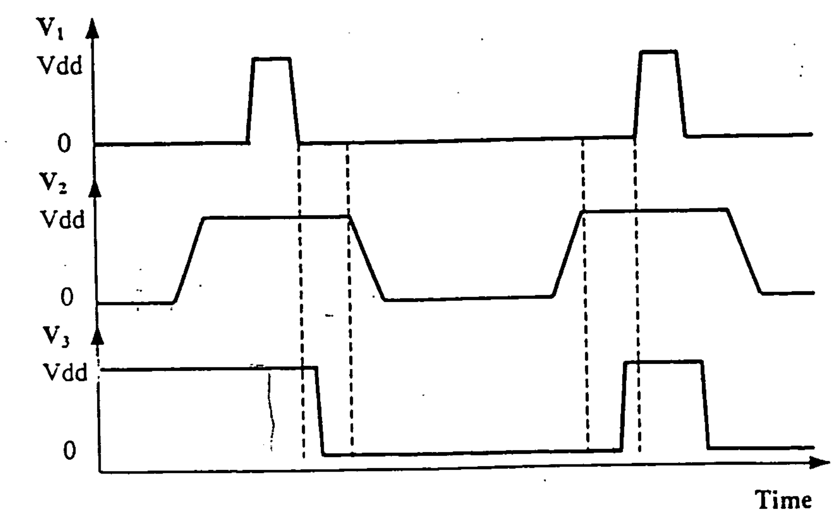
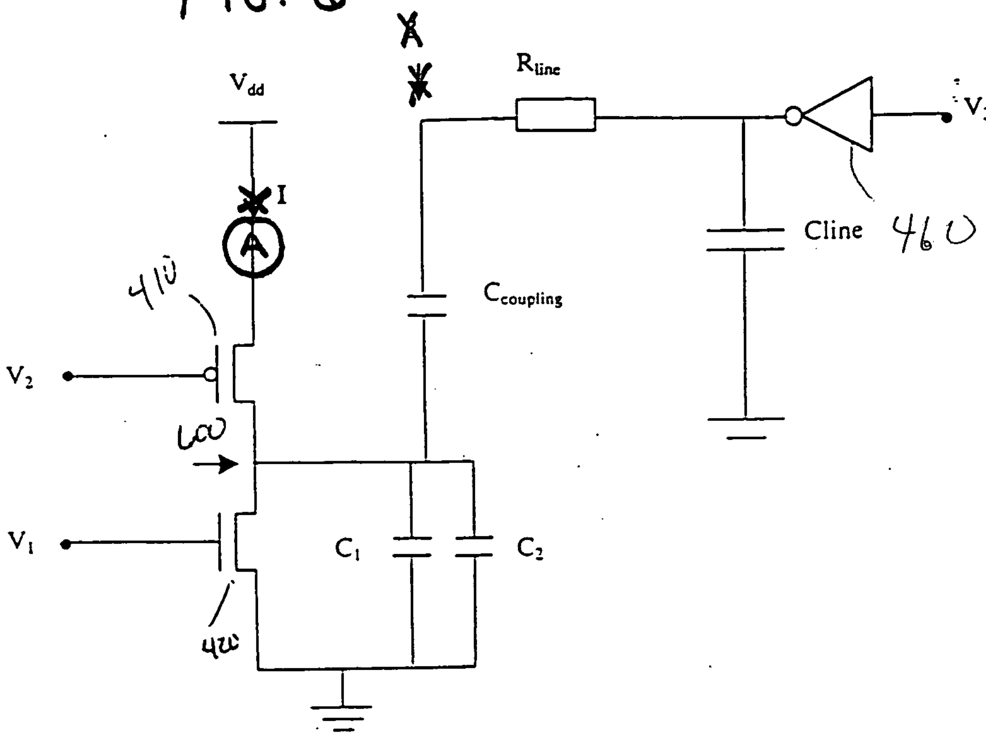


FIG. 5



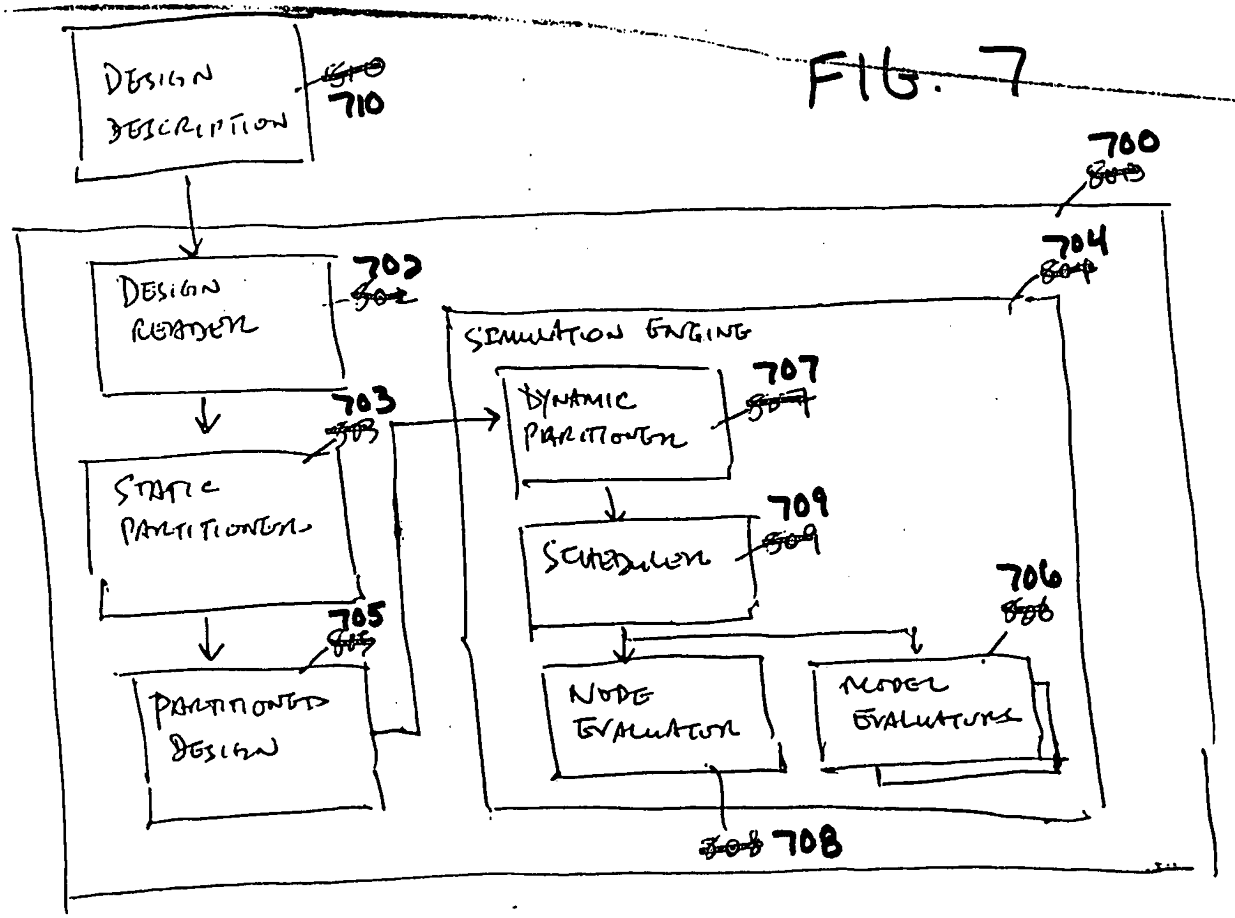
~~Fig. 5~~

FIG. 6



~~FIG. 6~~

FIG. 7


DESIGN DESCRIPTION
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700
~~800~~
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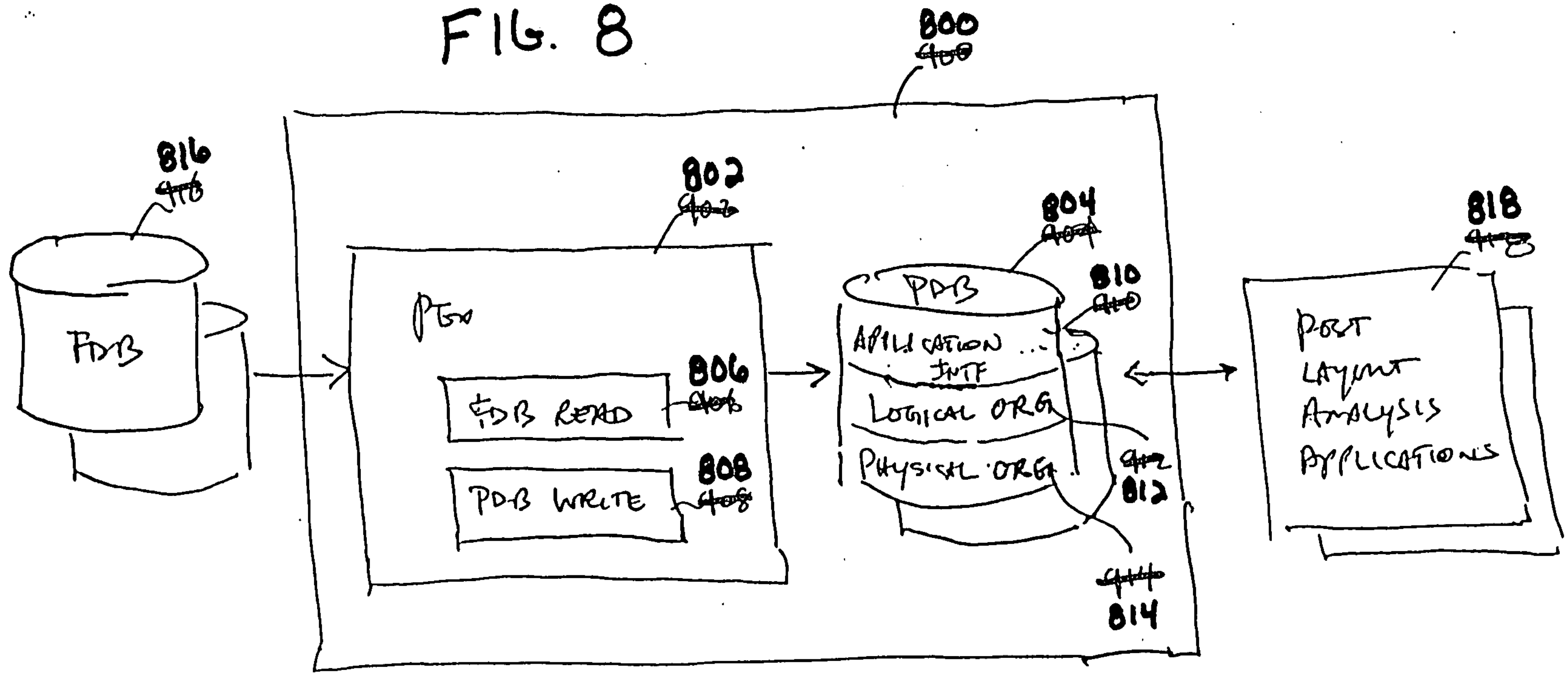
702
~~802~~
704
~~804~~
SIMULATION ENGINE
STATIC PARTITIONER
703
~~803~~
DYNAMIC PARTITIONER
707
~~807~~
SCHEDULER
709
~~809~~
PARTITIONED DESIGN
705
~~805~~
NODE EVALUATOR
MODEL EVALUATORS
706
~~806~~
~~808~~ 708

~~FIG. 8~~

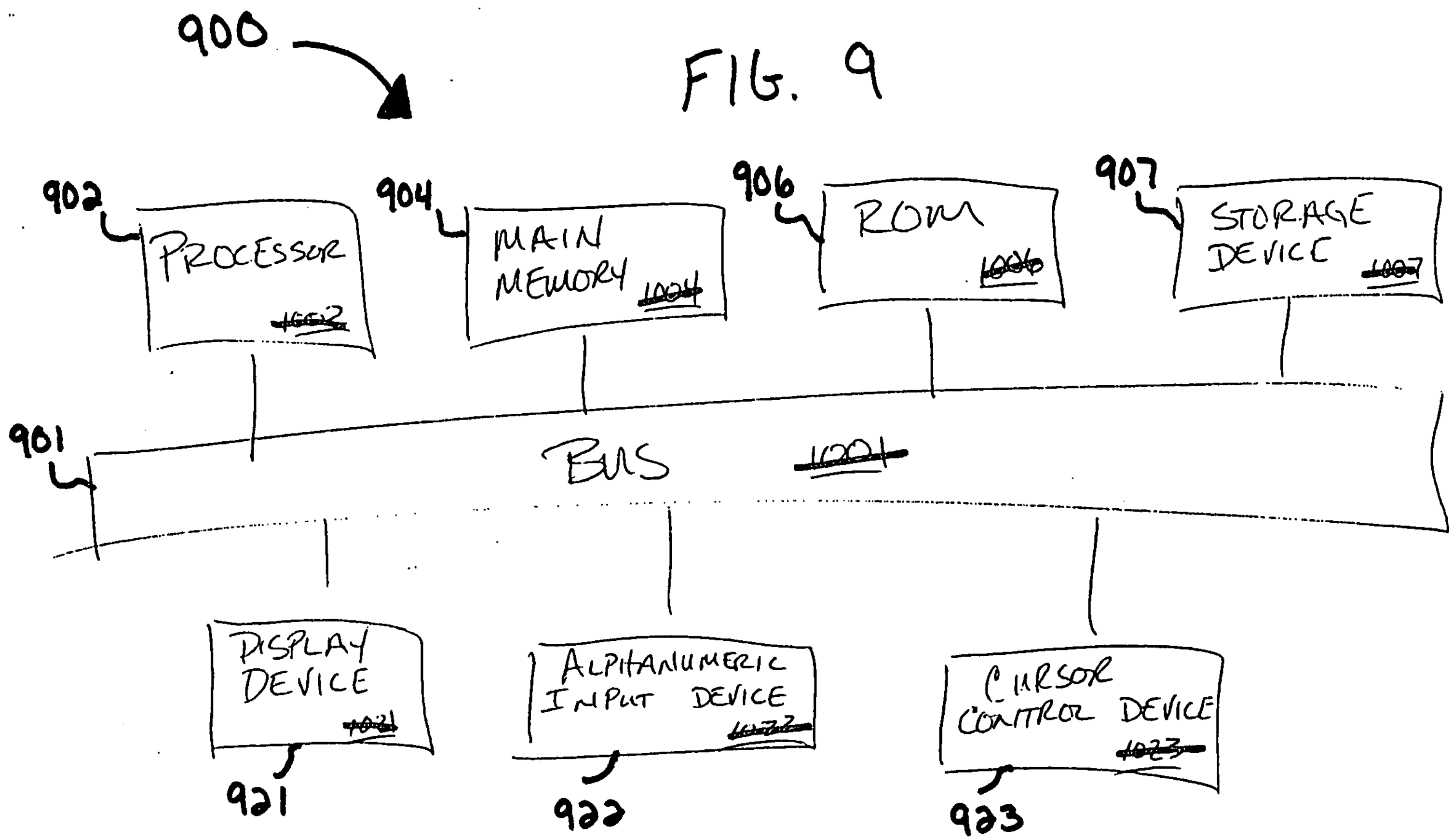
FIG. 8



~~FIGURE 4~~

~~1000~~

FIG. 9



~~FIG. 10~~